Two-Capacitor Transformer Winding Capacitance Models for Common-Mode EMI Noise Analysis in Isolated DC–DC Converters

Huan Zhang, Shuo Wang, *Senior Member, IEEE*, Yiming Li, *Student Member, IEEE*, Qinghai Wang, and Dianbo Fu

***Abstract*—For isolated dc–dc power converters, the interwinding parasitic capacitance of the transformer is usually one of the main paths for common-mode (CM) noise. In order to simplify the CM noise analysis, this paper proposes a two-capacitor transformer winding capacitance model. The model is derived based on general conditions so it can be applied to different isolated converter topologies. A measurement technique is also proposed to obtain the lumped capacitance for the model. The CM noise models of several isolated converter topologies are analyzed with the proposed two-capacitor transformer winding capacitance model to achieve simplicity. Finally, the proposed transformer winding capacitance model and measurement technique are verified by simulations and experiments.**

***Index Terms*—Common mode (CM), electromagnetic interference, isolated power converters, transformer winding capacitance model.**

NOMENCLATURE

v_P	Primary voltage of the transformer [V].
v_S	Secondary voltage of the transformer [V].
Δv_p	Voltage difference between two adjacent sections of the primary winding [V].
Δv_S	Voltage difference between two adjacent sections of the secondary winding [V].
L_{LK}	Transformer leakage inductance [H].
v_{Pi}	The voltage of section *i* on primary winding [V].
v_{Sj}	The voltage of section *j* on secondary winding [V].
C_{PiSj}	Interwinding parasitic capacitance between primary section *i* and secondary section *j* [F].
C_{PkPl}	Primary intrawinding parasitic capacitance between primary section *k* and *l* [F].
C_{SmSn}	Secondary intrawinding parasitic capacitance between secondary section *m* and *n* [F].
C_Q	The drain/collector to ground/heatsink parasitic capacitance of the MOSFET/insulated-gate bipolar transistor (IGBT) [F].
C_D	The cathode to ground/heatsink parasitic capacitance of the diode [F].
C_{QD}	A combination of C_Q and C_D [F].

Manuscript received September 7, 2016; revised November 29, 2016; accepted December 23, 2016. Date of publication January 10, 2017; date of current version June 23, 2017. This work was supported by Huawei Innovation Research Program. Recommended for publication by Associate Editor A. Lindemann. *(Corresponding author: D. Fu.)*

H. Zhang, S. Wang, and Y. Li are with the University of Florida, Gainesville, FL 32611 USA.

Q. Wang and D. Fu are with Huawei Technologies Co., Shenzhen 518057, China (e-mail: dianbo.fu@huawei.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2017.2650952

I. INTRODUCTION

DEVELOPING an accurate, simple, and efficient common mode (CM) noise model for dc–dc converters is very important for the analysis, prediction, and reduction of CM noise.

For isolated dc–dc power converters, the interwinding parasitic capacitance of the transformer is usually one of the main paths for CM noise [1]–[6]. A high-frequency (HF) transformer model is, therefore, the key for characterizing the CM noise. Several HF transformer modeling and parameter extraction methods have been proposed. However, many of them are not well suited for CM noise analysis. A little interest in the distribution of interwinding capacitances when building the model was payed in [7]–[11]. Their applications are mainly for examining the differential mode circuit dynamic behavior. Others are either too complicated [12]–[19] or vague [20]–[22] in how to determine the parasitic capacitances for different transformer structures, thus lack the ability for derivation of CM noise reduction techniques.

In order to facilitate the CM noise analysis, a CM noise model employing equivalent lumped capacitances to represent a real transformer which has distributed parasitic capacitances was proposed in [3], [4], [6]. One basic rule for the derivation of the lumped capacitance model is that the displacement current generated by the model must be equal to the actual transformer [4], [6]. As a result, the examination of the transformer's physical structure is unavoidable in all previous works. Due to the complexity of a real transformer, two assumptions are generally made to simplify the analysis. One assumption is that the voltage potential varies linearly along the windings; the other assumption is the parasitic capacitance between two adjacent windings is evenly distributed. Both assumptions linearize and simplify the displacement current calculation for a real transformer.

The modeling technique above works well for some transformers, especially for the transformers with spiral wire windings. However, it also has some issues. First, it is unclear why the displacement current instead of energy should be conserved during the model derivation. This actually defines a condition for the method to be used. Second, the two important assumptions needed for the derivation cannot be well held for some

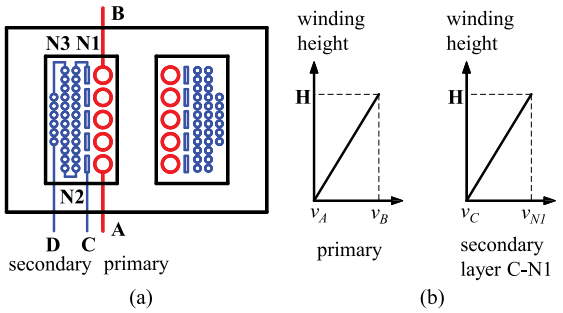


Fig. 1. (a) Typical transformer structure optimized for CM noise reduction and (b) the voltage distributions along winding layers.

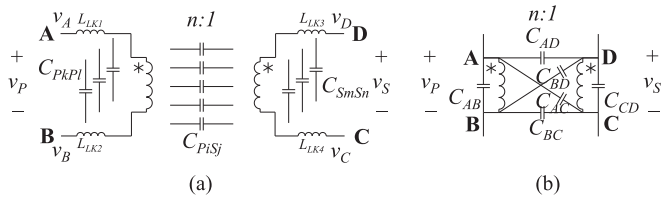


Fig. 2. CM winding capacitance modeling for a two-winding transformer.

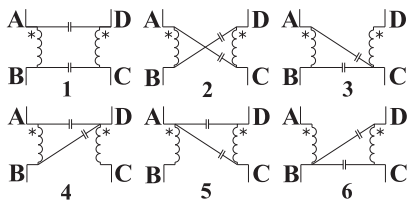


Fig. 3. Six possible two-capacitor CM winding capacitance models for a two-winding transformer.

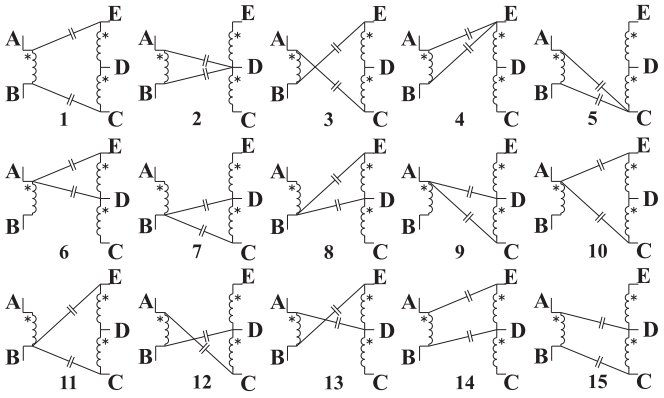


Fig. 4. Fifteen possible two-capacitor CM winding capacitance models for a center-tapped three-winding transformer.

transformer structures, especially for planar transformers with nonuniform winding layer profiles. Therefore, a new technique to extract the equivalent lumped capacitances without using these assumptions needs to be developed. Furthermore, the equivalent lumped capacitance model should be generalized for different isolated converter topologies. Xi *et al.* [6] did part of this work and were able to provide a general transformer model. The transformer winding capacitance is quantified and represented by four capacitances. However, the model derivation in the paper is still based on the two assumptions so it cannot be applied to a more general case.

This paper proposes a generalized two-capacitor transformer winding capacitance model for isolated power converters. Section II discusses existing techniques for solving the CM electromagnetic interference (EMI) issues of the isolated power converters. Section III derives the general constraints for the equivalent lumped capacitance transformer model using both the energy conservation rule and the displacement current conservation rule. A two-capacitor transformer winding capacitance model is then proposed based on the constraints of general applications. Section IV applies the proposed transformer model to different isolated converter topologies to demonstrate its flexibility and ability in the simplification of CM noise models. Section V proposes a measurement technique to extract the equivalent capacitances for the model. In Section VI, both an *LLC* resonant converter and a flyback converter are used to validate the proposed transformer model.

II. Existing CM Noise Analysis Methodologies for Isolated Power Converters

The interwinding capacitance of a transformer is one of the major paths for CM noise. This is mainly because of the high displacement currents due to the *dv/dt* added to the parasitic capacitances in the transformer. Additionally, interleaved winding structure is usually used to reduce winding loss. This increases the parasitic capacitance between the primary and secondary windings [4]. Furthermore, transformers tend to achieve low profiles and high power densities, so spiral wire windings may not be preferred. On the other hand, planar transformer is preferred since it is able to provide multiple benefits including low profile, good thermal characteristic, good repeatability, etc. [17]. Nevertheless, it has higher winding capacitance that generates higher CM noise than spiral wire winding transformer due to its closely stacked layers and intrinsically large layer surface areas.

There are two popular approaches to reduce the CM noise flowing through transformers [2], [6]. The basic principle of the first approach is to make sure that the adjacent primary and secondary winding layers have the same voltage distributions. It is assumed that the interwinding parasitic capacitances of the transformer are evenly distributed between these two adjacent winding layers, zero *dv/dt* can be maintained over these capacitances so no CM current is generated if there is no other parasitic capacitance between the primary and secondary winding layers.

Fig. 1(a) shows a transformer example for the flyback converter in Fig. 5(a) [2]. Winding AB is primary and winding CD is secondary. The primary layer and the secondary layer C-N1 have identical voltage distributions as shown in Fig. 1(b). It should be noted that line impedance stabilization networks (LISNs) are treated as short circuit for CM noise since their CM impedance is small compared with the impedance of transformer's parasitic capacitances. Because of this, both A and C terminals are equivalently connected to ground. v_A is approximately equal to v_C. So the *dv/dt* and the CM current between the two layers is zero. Apparently, the condition for

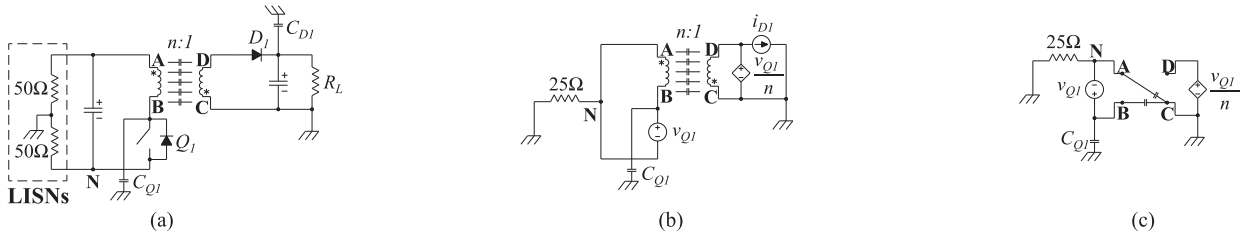


Fig. 5. CM model for a flyback converter: (a) converter circuit, (b) substitute nonlinear devices with voltage and current sources, and (c) final CM model.

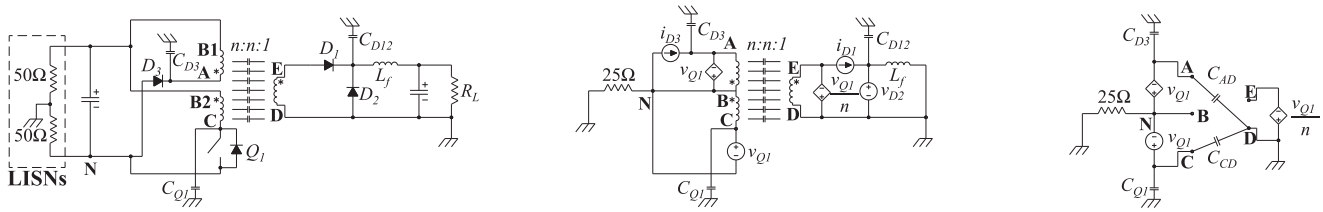


Fig. 6. CM model for a forward converter: (a) converter circuit, (b) substitute nonlinear devices with voltage and current sources, and (c) final CM model.

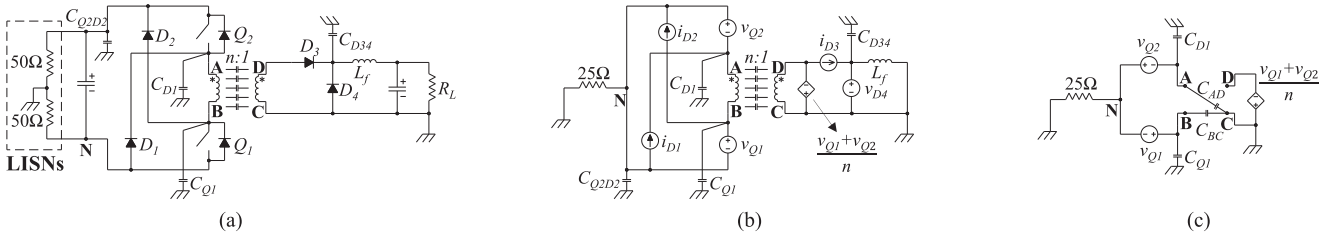


Fig. 7. CM model for a two-switch forward converter: (a) converter circuit, (b) substitute nonlinear devices with voltage and current sources, and (c) final CM model.

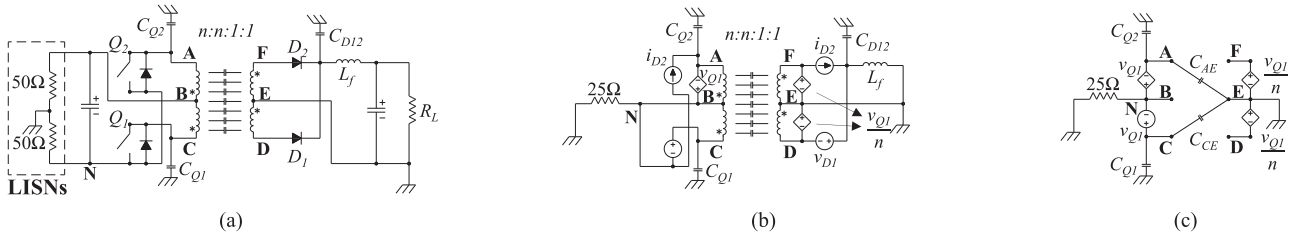


Fig. 8. CM model for a push-pull converter: (a) converter circuit, (b) substitute nonlinear devices with voltage and current sources, (c) final CM model.

this approach is that the voltage potential difference $v_A - v_C$ is always constant. For any power converter topologies meeting this condition, the approach can be applied to reduce the CM noise flowing through the transformer.

Following this rule, it has been identified that, besides flyback converter, this approach can also be applied to forward converter (see Fig. 6), push–pull converter (see Fig. 8), and half-bridge *LLC* resonant converter (see Fig. 9). However, for two-switch forward converter (see Fig. 7) and full-bridge *LLC* resonant converter (see Fig. 10) further examination is needed. It can be identified by the generalized equivalent noise source (ENS) method [6] that this approach does not work for any full-bridge converters with phase-shift control.

The effectiveness of the first approach is further limited when CM noise has more paths other than the transformer parasitic capacitance, e.g., the drain/collector to ground/heatsink parasitic capacitance of the MOSFET/IGBT. Furthermore, this approach only considers the parasitic capacitance between two adjacent layers. In some cases, when two layers are separated by a layer of thin or sparse winding such as the reset winding, the parasitic capacitance between these two layers cannot be ignored. Chu and Wang [5] consider these limitations and proposes a generalized CM current cancelation technique, which considers the CM noise from all CM paths. The technique was implemented on a forward converter and it also suggests that some transformer structures have better CM noise performance than

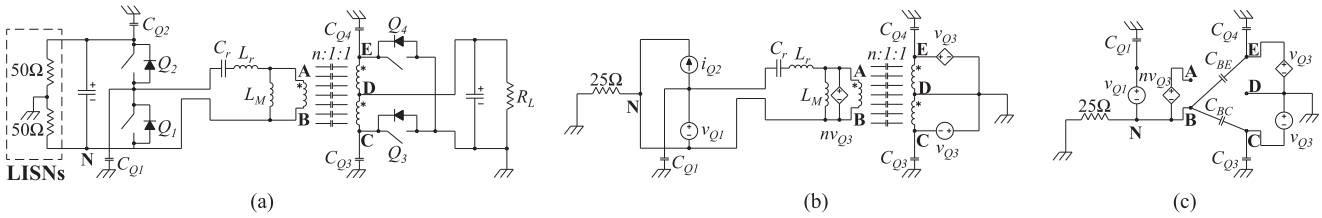


Fig. 9. CM model for a half-bridge LLC resonant converter: (a) converter circuit, (b) substitute nonlinear devices with voltage and current sources, and (c) final CM model.

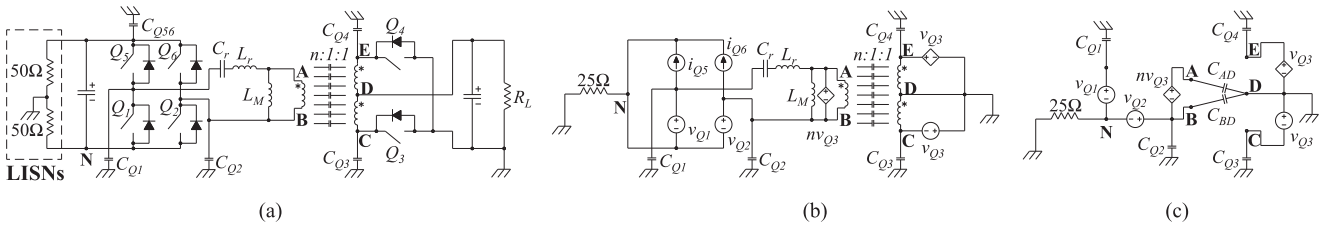


Fig. 10. CM model for a full-bridge LLC resonant converter: (a) converter circuit, (b) substitute nonlinear devices with voltage and current sources, and (c) final CM model.

others. However, it lacks the ability to predict the best transformer structure before the prototype is developed or its parasitic capacitances can be measured. Moreover, the first approach cannot be implemented in highly interleaved winding structures. Fu *et al.* [4] analyze a half-bridge *LLC* resonant converter with a fully interleaved planar transformer. Instead of implementing the first approach, the paper uses balance technique to reduce the CM noise.

The second approach is to first develop a transformer parasitic capacitance model based on its physical structure. Based on this model, various CM noise cancellation techniques, such as the balance technique [3], [4], [23], can be developed. Kong *et al.* [3] studies the CM noise balance technique for a two-switch forward converter based on its transformer parasitic capacitance model. According to displacement current conservation rule, Xie *et al.* [6] summarized the process to extract parasitic capacitance based on transformer physical structure.

Despite their effectiveness, Kong *et al.* [2]–[6] derived their key equations based on two important assumptions: 1) the voltage potential varies linearly along the windings; 2) the parasitic capacitances only exist between the adjacent layers and they are evenly distributed. It will be shown later that the displacement current conservation rule and the two assumptions limit the applications of using the existing lumped transformer winding capacitance model to reduce CM noise, so a more generalized approach needs to be developed.

III. Transformer Winding Capacitance Model

A good lumped winding capacitance model for a transformer is important for both CM noise simulation and analysis. Both [3] and [6] uses the displacement current conservation rule to develop lumped winding capacitance model for EMI analysis. First, it is unclear under what conditions the displacement current conservation rule holds for CM noise analysis. Second, it will be shown later that under some conditions, energy conservation rule instead of displacement current conservation rule should be used to derive transformer's lumped winding capacitance model. In this section, lumped winding capacitance models will be derived for transformers under general conditions. The conditions for both rules will be identified.

A. Transformer Winding Capacitance Model Based on Energy Conservation

Fig. 2(a) shows a two-winding transformer including its leakage inductances, inter- and intrawinding capacitances. Core loss and copper loss are not modeled as they are not important for EMI analysis. v_P and v_S are the primary and secondary voltages. L_{LK1}, L_{LK2} and L_{LK3}, L_{LK4} are primary and secondary leakage inductances, respectively. If the primary winding is separated to N sections from terminal B to A, and secondary winding is separated to M sections from terminal C to D with different voltages, the interwinding parasitic capacitance between primary section *i* and secondary section *j* is C_{PiSj}, where $i = 1, 2, \ldots,$ N and $j = 1, 2, \ldots,$ M. Similarly, C_{PkPl} is defined as the primary intrawinding capacitance between primary sections *k* and *l*, and C_{SmSn} is defined as the secondary intrawinding capacitance between secondary sections *m* and *n*, where *k* or *l* $= 1, 2, \ldots,$ N, and *m* or *n* $= 1, 2, \ldots,$ M.

If it is further defined that the voltage difference between any two adjacent sections is constant, Δv_P for primary winding, and Δv_S for secondary winding. They can be calculated as

$$\Delta v_P = \frac{v_P}{N-1} \tag{1}$$

$$\Delta v_S = \frac{v_S}{M-1}. \tag{2}$$

The voltages of section *i* on the primary winding and section *j* on the secondary winding are

$$v_{Pi} = v_B + (N-i)\Delta v_P \tag{3}$$

$$v_{Sj} = v_C + (M-j)\Delta v_S. \tag{4}$$

Two physically separated winding parts can be in the same section if their voltages are the same. For example, the equal potential parts of two paralleled windings that are interleaved by a secondary winding.

The energy stored in transformer's interwinding capacitances is

$$W_1 = \sum_{i=1}^{N}\sum_{j=1}^{M}\frac{1}{2}C_{PiSj}(v_{Pi}-v_{Sj})^2. \tag{5}$$

The energy stored in primary intrawinding capacitances is

$$W_2 = \sum_{k=1}^{N}\sum_{l=1}^{N}\frac{1}{2}C_{PkPl}(v_{Pk}-v_{Pl})^2. \tag{6}$$

The energy stored in secondary intrawinding capacitances is

$$W_3 = \sum_{m=1}^{M}\sum_{n=1}^{M}\frac{1}{2}C_{SmSn}(v_{Sm}-v_{Sn})^2. \tag{7}$$

And the total energy stored within parasitic winding capacitance is

$$W = W_1 + W_2 + W_3. \tag{8}$$

Based on (1)–(7), (8) can be represented as

$$W = \frac{1}{2}k_1(v_B-v_C)^2 + \frac{1}{2}k_2v_P^2 + \frac{1}{2}k_3v_S^2 + \frac{1}{2}k_4(v_B-v_C)v_P + \frac{1}{2}k_5(v_B-v_C)v_S + \frac{1}{2}k_6v_Pv_S \tag{9}$$

where

$$k_1 = \sum_{i=1}^{N}\sum_{j=1}^{M}C_{PiSj} \tag{10}$$

$$k_2 = \sum_{i=1}^{N}\sum_{j=1}^{M}C_{PiSj}\frac{N-i}{N-1} + \sum_{k=1}^{N}\sum_{l=1}^{N}C_{PkPl}\left(\frac{l-k}{N-1}\right)^2 \tag{11}$$

$$k_3 = \sum_{i=1}^{N}\sum_{j=1}^{M}C_{PiSj}\frac{M-j}{M-1} + \sum_{m=1}^{M}\sum_{n=1}^{M}C_{SmSn}\left(\frac{n-m}{M-1}\right)^2 \tag{12}$$

$$k_4 = 2\sum_{i=1}^{N}\sum_{j=1}^{M}C_{PiSj}\frac{N-i}{N-1} \tag{13}$$

$$k_5 = -2\sum_{i=1}^{N}\sum_{j=1}^{M}C_{PiSj}\frac{M-j}{M-1} \tag{14}$$

$$k_6 = -2\sum_{i=1}^{N}\sum_{j=1}^{M}C_{PiSj}\frac{N-i}{N-1}\cdot\frac{M-j}{M-1}. \tag{15}$$

The effect of leakage inductances is ignored in the analysis above as they significantly complicate the energy calculation. Because of this, the analysis in this paper applies to all the transformers with small leakage inductances. After leakage inductances are ignored, v_P and v_S meet condition

$$v_P = nv_S. \tag{16}$$

Substituting (16) into (9) yields

$$W = \frac{1}{2}k_1(v_B-v_C)^2 + \frac{1}{2}k_7(v_B-v_C)v_S + \frac{1}{2}k_8v_S^2 \tag{17}$$

where

$$k_7 = nk_4 + k_5 \tag{18}$$

$$k_8 = n^2k_2 + k_3 + nk_6. \tag{19}$$

Constants k_1, k_7, and k_8 are determined by transformer winding structure. Equation (17) shows that there are only two independent transformer terminal voltage differences: $v_B - v_C$ and v_S, in the calculation of the total energy stored in parasitic winding capacitance. This is reasonable as for all of the four terminal voltage differences v_P, v_S, $v_B - v_C$, and $v_A - v_D$, there are two constraints: (16) and the KVL, $v_P - v_S + (v_B - v_C) - (v_A - v_D) = 0$, so there are only two independent terminal voltage differences.

The simplest transformer winding capacitance model is the one with the least number of lumped capacitances. The derivation of the simplest model starts from a commonly used six-capacitor model in Fig. 2(b). The total energy stored in parasitic capacitances is

$$W = \frac{1}{2}(C_{AD}+C_{BD}+C_{AC}+C_{BC})(v_B-v_C)^2 + [(n-1)C_{AD} + nC_{AC} - C_{BD}](v_B-v_C)v_S + \frac{1}{2}\left[(n-1)^2C_{AD} + n^2C_{AC} + C_{BD} + n^2C_{AB} + C_{CD}\right]v_S^2. \tag{20}$$

The corresponding coefficients of (17) and (20) should be equal

$$\begin{cases} k_1 = C_{AD}+C_{BD}+C_{AC}+C_{BC} \\ \frac{1}{2}k_7 = (n-1)C_{AD} + nC_{AC} - C_{BD} \\ k_8 = (n-1)^2C_{AD} + n^2C_{AC} + C_{BD} + C_{INTRA} \end{cases}. \tag{21}$$

k_1 is the total capacitance between the primary and the secondary windings. C_{INTRA} is equal to $n^2C_{AB} + C_{CD}$. It is the total intrawinding capacitance reflected to the secondary side of the transformer. Because of this, the number of the lumped capacitances in the model is reduced from six to five. Furthermore, as there are only three constraints defined in (21), only three independent capacitances are enough for the transformer winding capacitance modeling with energy conservation. The other two are redundant and unnecessary. For example, C_{INTRA}, C_{AD}, C_{AC} or C_{AD}, C_{AC}, C_{BD} can be used to develop the model and the other two can be just set to zero. There are ten possible combinations in total.

B. Transformer Winding Capacitance Model Based on Displacement Current Conservation

Since the CM noise displacement current only flows through interwinding capacitances of the transformer, the derivation of the transformer winding capacitance model based on displacement current conservation will not have intrawinding capacitances involved.

Based on Fig. 2(a), the CM noise displacement current flowing between two windings can be calculated by

$$i_{CM} = \sum_{i=1}^{N}\sum_{j=1}^{M} C_{PiSj}\frac{d(v_{Pi}-v_{Sj})}{dt}. \tag{22}$$

Substituting (1)–(4) into (22) yields

$$i_{CM} = \sum_{i=1}^{N}\sum_{j=1}^{M} C_{PiSj}\frac{d(v_B-v_C)}{dt} + \sum_{i=1}^{N}\sum_{j=1}^{M} C_{PiSj}\frac{N-i}{N-1}\frac{dv_P}{dt} - \sum_{i=1}^{N}\sum_{j=1}^{M} C_{PiSj}\frac{M-j}{M-1}\frac{dv_S}{dt}. \tag{23}$$

Since the leakage inductances are ignored, (16) can be used to further simplify (23) to

$$i_{CM} = \sum_{i=1}^{N}\sum_{j=1}^{M} C_{PiSj}\frac{d(v_B-v_C)}{dt} + \sum_{i=1}^{N}\sum_{j=1}^{M}\left(n\frac{N-i}{N-1}-\frac{M-j}{M-1}\right)C_{PiSj}\frac{dv_S}{dt}. \tag{24}$$

Substituting (10), (13), (14) and (18) into (24) yields

$$i_{CM} = k_1\frac{d(v_B-v_C)}{dt} + \frac{1}{2}k_7\frac{dv_S}{dt}. \tag{25}$$

Again, if the derivation of the simplest model starts from the six-capacitor model in Fig. 2(b), the CM current can be expressed as

$$i_{CM} = (C_{AD}+C_{AC}+C_{BD}+C_{BC})\frac{d(v_B-v_C)}{dt} + [(n-1)C_{AD}+nC_{AC}-C_{BD}]\frac{dv_S}{dt}. \tag{26}$$

The corresponding coefficients of (25) and (26) are equal

$$\begin{cases} k_1 = C_{AD}+C_{AC}+C_{BD}+C_{BC} \\ \frac{1}{2}k_7 = (n-1)C_{AD}+nC_{AC}-C_{BD} \end{cases}. \tag{27}$$

Because there are only two constraints in (27), obviously, two independent capacitances are enough to model the transformer winding capacitance with displacement current conservation. The other two capacitances can be set to zero. For example, if C_{AC} and C_{BC} are set to zero, $k_1 = C_{AD}+C_{BD}$.

C. Discussions on the Results From Two Rules

Comparing (21) and (27), the first two constraints are identical and they are determined by the interwinding capacitances only. The energy conservation results in one more constraint that reflects the effect of intrawinding capacitance. So it can correctly characterize both inter- and intrawinding capacitances, whereas the displacement current conservation cannot characterize the intrawinding capacitance.

Although CM noise current is directly related to the interwinding capacitance, depending on the converter topologies, the intrawinding capacitance may influence the CM noise by influencing the waveforms of voltage v_A, v_B, v_C, and v_D. Equation (21) derived from the energy conservation is, therefore, more preferred for CM noise analysis and simulations than (27) derived from displacement current conservation for some converter topologies.

When an independent voltage source is directly connected to a transformer terminal, the intrawinding capacitances have no influence to the voltage waveform of that terminal since it is in parallel with the voltage source.

D. Two-Capacitor Transformer Winding Capacitance Model

Based on the analysis above, when two conditions below are met, the transformer winding capacitance can be modeled with two capacitors:

1) the transformer's leakage inductance is small so its effect can be ignored;
2) at least one winding of the transformer are connected to an equivalent independent voltage source. This source can be the equivalent voltage source used to substitute nonlinear switches [23].

Condition 1) ensures that the three constraints derived by energy conservation in (21) are valid. The transformer winding capacitance is able to be represented with one intrawinding capacitance and two interwinding capacitances. Condition 2) ensures that the intrawinding capacitance is in parallel with an independent voltage source so it can be removed in noise analysis. Therefore, only two interwinding capacitors are needed to represent transformer winding capacitance. The extraction of the two interwinding capacitances will be discussed later.

As shown in Fig. 3, there are six possible two-capacitor winding capacitance models for a two-winding transformer. For a center-tapped three-winding transformer, its two-capacitor winding capacitance model can be derived based on the same process as a two-winding transformer. The resulting models can be found in Fig. 4. The total number of possible models is $C_6^2 = 6\times 5/2 = 15$. Since the center-tapped three winding transformer can be treated as a two-winding transformer with one added terminal in the center, two capacitances are still enough for the model.

E. Influence of Leakage Inductance on the Model

The influence of leakage inductance becomes significant when the frequency is high due to its increased impedance. Therefore, the boundary frequency below which the proposed transformer model is good for CM EMI analysis can be approximately evaluated and calculated based on the resonant frequency between the leakage inductance and the total interwinding parasitic capacitance of the transformer k_1. In Fig. 2(a), under normal conditions, $L_{LK1}\approx L_{LK2}$, $L_{LK3}\approx L_{LK4}$, the resonant

frequency between the leakage inductance and k_1 is calculated as

$$f_{CM} \approx 1/\left[2\pi\sqrt{(L_{LK1}+L_{LK3})k_1}\right]. \quad (28)$$

Below f_{CM}, the model is good for CM noise analysis because the leakage inductance's impedance can be ignored as it is much smaller than k_1's impedance. Above f_{CM}, the model becomes less effective as the impedance of the leakage inductance is dominant on the CM noise's path in the transformer. In many cases, f_{CM} is high enough to cover most of the concerned frequency range (150 kHz to 30 MHz). Sometimes, circuit designers intentionally increase transformer's leakage inductance so it can be used as a resonant inductance in resonant converters. If that is the case, researchers should always use (28) to check if the proposed model can still be applied to CM noise analysis.

IV. Applications of the Two-Capacitor Transformer Winding Capacitance Model to CM Noise Analysis

The advantage of the proposed two-capacitor transformer winding capacitance model lies in its flexibilities for the analysis and cancellation of the CM noise caused by transformer winding capacitances. Along with the substitution theory that was first used for noise analysis in [8], it has the ability to greatly simplify the CM noise model for isolated power converters.

The applications of the two-capacitor winding capacitance model to the CM analysis of the conventional isolated power converters are shown from Figs. 5 to 10. In these figures, C_Q represents the drain/collector to ground/heatsink parasitic capacitance of the MOSFET/IGBT. C_D represents the cathode to ground/heatsink parasitic capacitance of the diode. C_{QD} includes both C_Q and C_D.

The derivation of the CM noise models based on two-capacitor winding capacitance model for the analysis of the CM noise caused by transformer winding capacitances follows seven steps below.

1) Substitute nonlinear semiconductor devices with either equivalent voltage sources or currents sources using substitution theory. The voltage and current sources shall have the same time domain waveforms as the originals. Using either voltage sources or currents sources depends on the convenience in noise analysis [5]. The input and output bulk dc capacitors are treated as short circuit because they have very small impedance to CM noise.
2) If one transformer winding is paralleled with a voltage source, replace all other windings with controlled voltage sources because the winding voltages depend on transformer turn ratios.
3) Simplify the model by removing all components that are in parallel with the voltage sources or in series with current sources.
4) Use one of the models that most simplifies the CM noise analysis in Figs. 3 or 4 to replace the original transformer.
5) Analyze the CM noise generated by every voltage source and current source based on superposition theory.
6) Remove the parasitic capacitances that do not contribute to the CM noise flowing through LISNs by analyzing the circuit derived from step 1 to 5.
7) Analyze CM noise based on the resultant CM noise models developed from step 1 to 6.

Step 4 is very important as it is directly related to CM noise analysis and cancellation techniques. This paper will employ examples to show how to use the two-capacitor transformer winding capacitance model to simplify the CM noise analysis. Based on the developed CM EMI model, it is easy to derive techniques for CM noise cancellation.

A. Flyback Converter

Following steps 1 and 2, the flyback converter in Fig 5(a) can be transformed to Fig. 5(b). Following steps 3–6, i_{D1} does not contribute to CM noise and final CM model is derived in Fig. 5(c). In step 4, the model 3 in Fig. 3 is selected as transformer model because with this model, V_{Q1}/n on the secondary does not contribute to CM noise. Furthermore, there is no current flowing through C_{AC} as the LISNs' impedance is much smaller than that of C_{Q1}. The condition for CM noise cancellation is $C_{BC} = -C_{Q1}$. Negative capacitance is mathematically possible in transformer models.

B. Forward Converter

Following steps 1 and 2, the forward converter in Fig 6(a) can be transformed to Fig. 6(b). Following steps 3–6, i_{D1}, v_{D2}, and i_{D3} do not contribute to CM noise, and final CM model is derived in Fig. 6(c). In Fig. 6(c), since C_{AD} and C_{CD} are both connected to the secondary ground, V_{Q1}/n on the secondary does not contribute to CM noise. The voltages between N and A, C and N are both v_{Q1}. If $C_{D3} = C_{Q1}$, $C_{AD} = C_{CD}$, the CM currents can be canceled.

C. Two-Switch Forward Converter

Following steps 1 and 2, the two-switch forward converter in Fig 7(a) can be transformed to Fig. 7(b). Following steps 3–6, i_{D1}, i_{D2}, i_{D3}, and v_{D4} do not contribute to CM noise and the final CM model is derived in Fig. 7(c). The final CM model is similar to that of the forward converter in Fig. 6(c). Based on the operation principle of two-switch forward converter, ideally, v_{Q1} and v_{Q2} have identical waveforms. If $C_{D1} = C_{Q1}$, $C_{AC} = C_{BC}$, the CM currents are canceled.

D. Push–Pull Converter

Although the topology in Fig. 8(a) is very different from the forward converter in Fig. 6(a), the final CM model for push–pull converter with the two-capacitance transformer model in Fig. 8(c) is similar to that of a forward converter. The condition to cancel CM noise is $C_{Q1} = C_{Q2}$, $C_{AE} = C_{CE}$.

E. Half-Bridge LLC Resonant Converter

For the half-bridge *LLC* resonant converter in Fig. 9(a), following steps 1 and 2, the CM noise model in Fig. 9(b) can be derived. Following steps 3–6, i_{Q2} does not contribute to CM

noise and the final CM model is derived in Fig. 9(c). As shown in Fig. 9(c), for the half-bridge *LLC* resonant converter, the two capacitances C_{BE} and C_{BC} are selected to take advantage of two identical secondary voltages and the transformer primary voltage nv_{Q3} can be ruled out in CM noise analysis. If the CM noise generated by C_{Q1} can be ignored, the condition for CM noise cancellation is $C_{BE} = C_{BC}$.

F. Full-Bridge LLC Resonant Converter

For the full-bridge *LLC* resonant converter in Fig. 10(a), following steps 1 and 2, the CM noise model in Fig. 10(b) can be derived. Following steps 3–6, i_{Q5} and i_{Q6} do not contribute to CM noise and the final CM model is derived in Fig. 10(c). Theoretically, based on the operating principle of full-bridge *LLC* resonant converters, $v_{Q1} = -v_{Q2}$. It is also assumed that the switching frequency is equal or very close to the resonant frequency, so $nv_{Q3} \approx v_{Q1} - v_{Q2}$. Because the output is grounded, independent and dependent voltage sources v_{Q3} do not contribute to CM noise. C_{Q3} and C_{Q4} are shorted by the output grounding. Based on these relationships, the condition for CM cancellation is $C_{Q1} = C_{Q2}$ and $C_{AD} = C_{BD}$.

It should be pointed out that the converter outputs in Figs. 5–10 are grounded. If they are not grounded, the CM noise analysis and the conditions for CM noise cancellation could be different. The techniques developed in this paper still apply.

V. Extraction of Capacitances for Two-Capacitor Transformer Winding Capacitance Models

In this section, the relationship of different transformer models in Figs. 3 and 4 will be first discussed. An extraction technique is proposed to determine the capacitances in the transformer models.

A. Relationship of Different Two-Capacitor Transformer Winding Capacitance Models

Since the intrawinding capacitance of the transformer can be removed in CM EMI analysis when an independent voltage source is added to one terminal of the transformer, the two-capacitor transformer winding capacitance model only characterize the interwinding capacitance; that is to say, all the models in Figs. 3 and 4 are only limited by the first two constraints in (21). These models lead to identical CM noise. Displacement current rule can be used to find their relationships since it has enough information in defining the interwinding capacitance.

If models 2 and 11 in Fig. 4 are taken as examples, the displacement CM currents derived from the two models are

$$i_{CM} = C_{AD}\frac{dv_{AD}}{dt} + C_{BD}\frac{dv_{BD}}{dt} \tag{29}$$

$$i_{CM} = C_{BE}\frac{dv_{BE}}{dt} + C_{BC}\frac{dv_{BC}}{dt}. \tag{30}$$

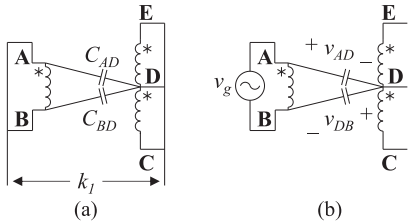


Fig. 11. Extract the capacitances for transformer winding capacitance model: (a) measure the total primary to secondary capacitance k_1, and (b) measure the voltage ratio between v_{AD} and v_{DB}.

If the turn ratio of the transformer is *n*:1:1, v_{AD}, v_{BE}, and v_{BC} can be expressed as

$$v_{AD} = v_{AB} + v_{BD} = nv_{ED} + v_{BD} \tag{31}$$

$$v_{BE} = v_{BD} - v_{ED} \tag{32}$$

$$v_{BC} = v_{BD} + v_{DC} = v_{BD} + v_{ED}. \tag{33}$$

Substituting (31)–(33) into (29) and (30) yields

$$i_{CM} = (C_{AD} + C_{BD})\frac{dv_{BD}}{dt} + nC_{AD}\frac{dv_{ED}}{dt} \tag{34}$$

$$i_{CM} = (C_{BC} + C_{BE})\frac{dv_{BD}}{dt} + (C_{BC} - C_{BE})\frac{dv_{ED}}{dt}. \tag{35}$$

By comparing the coefficients of (34) and (35), the relationship of the capacitances in these two models is

$$\begin{cases} C_{BE} = \frac{(1-n)C_{AD}+C_{BD}}{2} \\ C_{BC} = \frac{(1+n)C_{AD}+C_{BD}}{2} \end{cases}. \tag{36}$$

If $C_{BD}/C_{AD} = h$

$$\frac{C_{BC}}{C_{BE}} = \frac{h+1+n}{h+1-n}. \tag{37}$$

The capacitance relationship of other models can be derived similarly. If the capacitances of one model are extracted, the capacitances of all other models can be calculated.

B. Extraction of Capacitances for Transformer Models

Equation (37) indicates that if the capacitance ratio $C_{BD}/C_{AD} = h$ can be directly measured, the ratio from C_{BC} to C_{BE} can be calculated from *n* and *h*. Similarly, the capacitance ratio of any two capacitances in other models in Fig. 4 can also be derived.

The model 2 in Fig. 4 is taken as an example for the proposed parasitic capacitance extraction technique in Fig. 11. In Fig. 11 (a), primary terminals and secondary terminals are first shorted. The total primary to secondary capacitance k_1, which is defined in (21) and (27), is then measured using an impedance analyzer. In Fig. 11(b), a signal generator is added to the primary winding. The voltage v_{AD} between terminals A and D and the voltage v_{DB} between terminals D and B are measured using an oscilloscope or a voltmeter. If the capacitance of the voltage probes of the oscilloscope or the voltmeter can be ignored, C_{AD} and

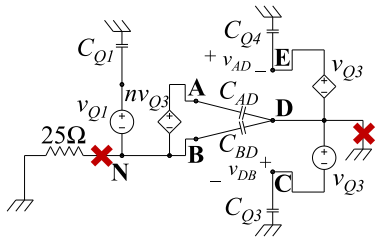


Fig. 12. Extract C_{AD} and C_{BD} for a half-bridge LLC resonant converter under working condition.

C_{BD} can be solved by (38)

$$\begin{cases} C_{BD} = k_1 \frac{v_{AD}}{v_g} \\ C_{AD} = k_1 \frac{v_{DB}}{v_g} \end{cases}. \tag{38}$$

Otherwise the probe capacitance should be considered in the calculation. The capacitances of all other models can be calculated based on their relationships, which can be derived following the procedure in Section V-A with C_{AD} and C_{BD}.

For the CM model of a half-bridge *LLC* converter in Fig. 12, the capacitances C_{AD} and C_{BD} can also be extracted by directly measuring the voltage v_{AD} between terminals A and D and the voltage v_{DB} between terminals D and B at working conditions if C_{Q1}, C_{Q3} and C_{Q4} are much smaller than C_{AD} and C_{BD}.

In Fig. 12, if both the input and the output of the converter are disconnected from the ground, the measured working waveforms for v_{AD} and v_{DB} under converter working conditions will be determined by nv_{Q3}, C_{AD} and C_{BD}. So C_{AD} and C_{BD} can still be calculated from (38) with $v_g = nv_{Q3}$.

VI. Simulation and Experimental Verification

A. Verification With an LLC Resonant Converter

Experimental verification is first conducted with a 1 kW full-bridge *LLC* resonant converter in Fig. 10 with both input and output ungrounded. The input and output rated voltages are 48 and 12 V, respectively. The switching frequency is 910 kHz. C_{AD} and C_{BD} are much larger than other capacitances in the model, so the influence of other capacitances can be ignored in the measurements.

In order to verify the two-capacitor transformer winding capacitance model and the capacitance extraction technique, two measurements are conducted based on the models 2 and 11 in Fig. 4. Fig. 13(a) is the measured voltage waveforms of v_{AD} and v_{DB}. The ratio $h \approx 1.5$ was calculated from the magnitudes of the voltages. According to (37), as the transformer turn ratio is 4:1:1, it is predicted that $C_{BC}/C_{BE} = v_{EB}/v_{BC} \approx -4.3$. From the measured voltage magnitudes in Fig. 13(b), it is shown that the measured results match the predicted very well.

The total capacitance k_1 can be measured as 4.2 nF by shorting the primary terminals and secondary terminals of the transformer shown in Fig. 11(a). C_{BD} and C_{AD} are calculated from (38) as 1.68 and 2.52 nF.

By performing a CM EMI noise prediction, the proposed transformer modeling technique can be further verified. The

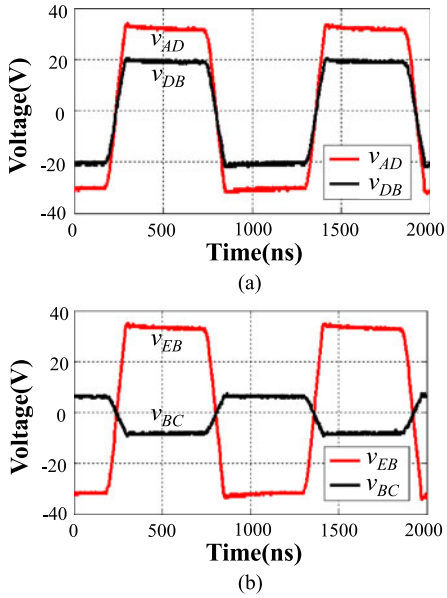


Fig. 13. Measured working voltages: (a) v_{AD} and v_{DB}, and (b) v_{EB} and v_{BC}.

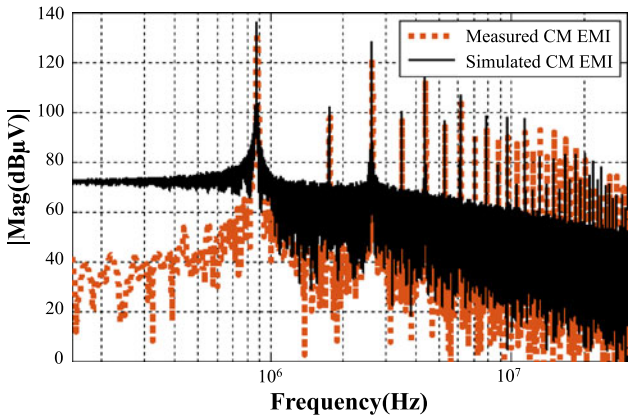


Fig. 14. Comparison of the simulated and measured CM noise spectra of the LLC resonant converter.

CM spectrum is simulated with the transformer model in Fig. 10(c) and the extracted parameters when both input and output are grounded. Noise sources v_{Q1}, v_{Q2}, and v_{Q3} used in simulation are directly from the measured voltage waveforms with an oscilloscope. Fig. 14 shows the comparison between the simulated and measured noise spectra. The noise spikes match well especially in low-frequency range. The background noise of the measured noise is related to the experiment environment and the spectrum analyzer settings. The simulated background noise is related to the sampling rate and the number of fast Fourier transform points. These two normally do not match. However, this does not influence EMI analysis.

As analyzed previously, if C_{AD} is equal to C_{BD}, the CM noise can be reduced. This is achieved by paralleling a 0.84 nF capacitor between A and D in the experiment. A 25 dB CM noise reduction is achieved at the switching frequency in the measured EMI in Fig. 15. This verifies the analysis in the paper.

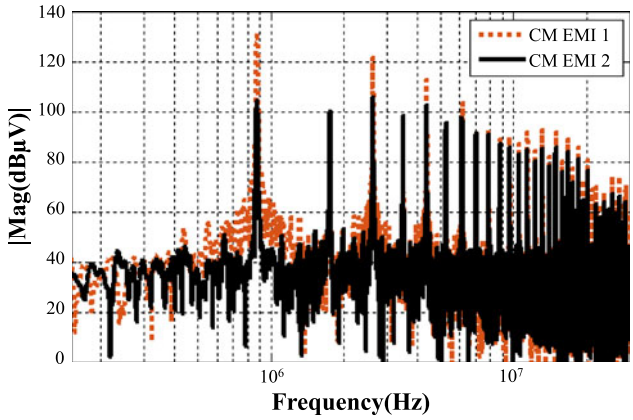


Fig. 15. Comparison of the measured CM noise spectra of the LLC resonant converter before (CM EMI 1) and after (CM EMI 2) CM noise cancellation.

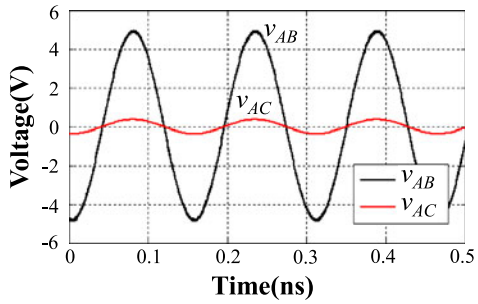


Fig. 16. Measured v_{AB} and v_{AC} of a flyback transformer with a signal generator and an oscilloscope.

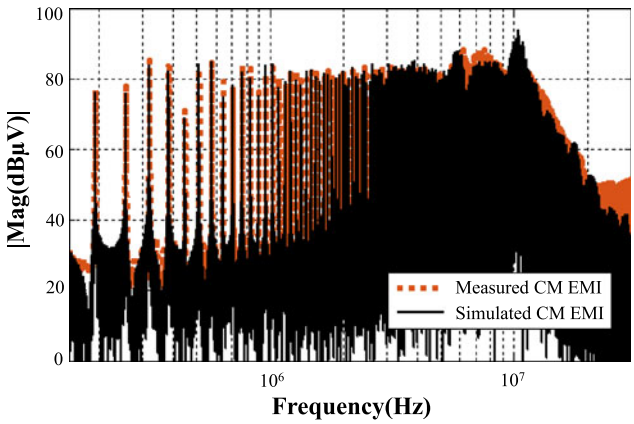


Fig. 17. Comparison of the simulated and measured CM noise spectra of the flyback converter.

B. Verification With a Flyback Converter

The second experimental verification is conducted with a 45 W ac/dc flyback converter. Its input voltage is 120 VAC. Its output voltage is 12 VDC. It has a switching frequency 65 kHz. A diode bridge is located between the LISNs and the input dc capacitor in Fig. 5(a). The CM noise model is similar to that in Fig. 5(c) except that the LISN's 25 Ω impedance should be replaced with the total impedance of the CM impedance of the diode bridge and the LISN's 25 Ω impedance because they are in series in the CM noise path. The CM impedance of the diode bridge is very small when one or two diodes conduct currents.

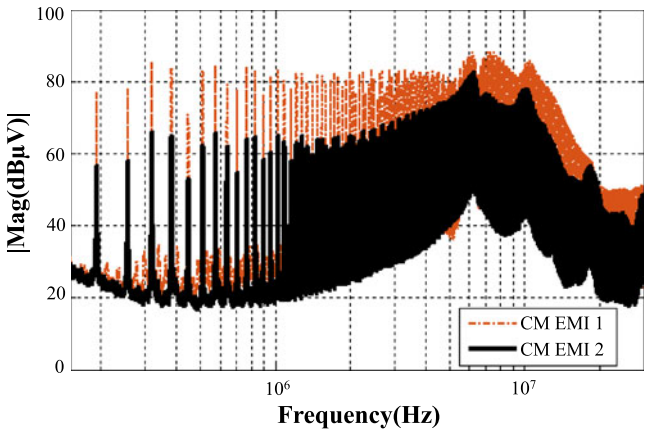


Fig. 18. Comparison of the measured CM noise spectra of the flyback converter before (CM EMI 1) and after (CM EMI 2) CM noise cancellation.

When all diodes are OFF, it is determined by the junction capacitance of the diodes so it is big. The condition for CM noise cancellation is, therefore, still $C_{BC} = -C_{Q1}$

C_{AC} and C_{BC} can be measured similarly to that in Fig. 11 except that the secondary has only one winding. The total capacitance k_1 is measured as 110 pF by shorting the primary terminals and secondary terminals of the transformer. To extract C_{AC} and C_{BC}, a 65 kHz, 10 V_{p-p} sinusoidal signal is added to the primary winding with a signal generator having 50O-hm source impedance. The voltages v_{AB} and v_{AC} are measured with an oscilloscope. Because the voltage probes of the oscilloscope have capacitance $C_{probe} = 22$ pF, whose effects on voltage measurement cannot be ignored, when calculating C_{AC} and C_{BC}, C_{probe} must be considered. On the other hand, since C_{BC} and C_{BE} are much larger than C_{probe} in Fig. 13, C_{probe}'s effect is ignored in Fig. 13.

Fig. 16 is the measured time-domain waveforms for v_{AB} and v_{AC}. From the measurement, it is found that $v_{AC}/v_{AB} = C_{BC}/(k_1 + C_{Probe}) \approx 0.072$. C_{BC} is then calculated as 9.5 pF. C_{AC} equals to $(k_1 - C_{BC})$ and is calculated as 100.5 pF. In this flyback converter, the heatsink of the main MOSFET switch is connected to the primary ground. Therefore, $C_{Q1} = 0$.

To verify the proposed transformer model, CM noise prediction and reduction were conducted for the flyback converter. The CM spectrum is simulated with the transformer model in Fig. 5(c) and the extracted parameters when both input and output are grounded. Noise source v_{Q1} used in the simulation are directly from the measured voltage waveforms with an oscilloscope. In Fig. 17, a simulated CM noise spectrum is compared with the measured one. The two matches quite well in general. The mismatch above 6 MHz is due to other high-frequency parasitic parameters that is not modeled in Fig. 5(c) in the CM noise loop.

Since $C_{Q1} = 0$, the 9.5 pF C_{BC} should be canceled to cancel CM noise. This can be achieved by adding a capacitor between D and A to generate a reverse CM current to cancel the CM noise from B to C. Because the turns ratio $n = 5$, a 47-pF capacitor is used for cancellation.

The measured CM EMI noise spectra before and after adding the compensation capacitor are shown in Fig. 18. It is shown

that after the compensation, a maximum 18-dB noise reduction is achieved from 150 kHz to above 10 MHz, which verifies the effectiveness of the proposed modeling and noise reduction techniques.

VII. Conclusion

This paper proposes a transformer winding capacitance modeling technique for the CM EMI analysis in isolated power converters. The developed modeling technique has multiple benefits:

1) it is derived based on general conditions, thus, it has a wide range of applications for CM noise analysis and cancelation;
2) the lumped capacitances of the model can be obtained by simple measurements;
3) the model has great flexibility in simplifying the CM EMI circuit model. The developed technique was validated with both simulations and experiments.

With the help of the proposed model, researchers and engineers can free themselves from the examination of transformer physical structures when analyze the CM EMI performance of isolated converters. As long as the conditions defined in the paper are met, the developed two-capacitor model can always be applied to the transformer modeling for CM noise analysis. The proposed lumped capacitance extraction technique for the developed model is not only easy to use but also able to evaluate transformer's CM characteristics in many applications. Designers can easily make a balanced transformer with the proposed capacitance extraction technique.

References

[1] B. Yang, F. C. Lee, A. J. Zhang, and G. Huang, "LLC resonant converter for front end DC/DC conversion," in *Proc. 17th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2002, pp. 1108–1112.

[2] P. J. Kong and F. C. Lee, "Transformer structure and its effects on common mode EMI noise in isolated power converters," in *Proc. 25th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2010, pp. 1424–1429.

[3] P. J. Kong, S. Wang, F. C. Lee, and Z. J. Wang, "Reducing common-mode noise in two-switch forward converter," *IEEE Trans. Power Electron.*, vol. 26, no, 5, pp. 1522–1533, May 2011.

[4] D. B. Fu, S. Wang, P. J. Kong, F. C. Lee, and D. C. Huang, "Novel techniques to suppress the common-mode EMI noise caused by transformer parasitic capacitances in DC-DC converters," *IEEE Trans. Ind. Electron.*, vol. 60, no. 11, pp. 4968–4977, Nov. 2013.

[5] Y. B. Chu and S. Wang, "A generalized common-mode current cancelation approach for power converters," *IEEE Trans. Ind. Electron.*, vol. 62, no. 7, pp. 4130–4140, Jul. 2015.

[6] L. H. Xie, X. B. Ruan, and Z. H. Ye, "Equivalent noise source: An effective method for analyzing common-mode noise in isolated power converters," *IEEE Trans. Ind. Electron.*, vol. 63, no. 5, pp. 2913–2924, May 2016.

[7] A. Baccigalupi, P. Daponte, and D. Grimaldi, "On circuit theory approach to evaluate the stray capacitances of two coupled inductors," in *Proc. Instrum. Meas. Technol. Conf.*, 1993, pp. 549–553.

[8] H. Y. Lu, J. G. Zhu, V. S. Ramsden, and S. Y. R. Hui, "Measurement and modeling of stray capacitances in high frequency transformers," in *Proc. 30th Annu. IEEE Power Electron. Spec. Conf.*, 1999, vol. 2, pp. 763–768.

[9] H. Y. Lu, J. G. Zhu, and S. Y. R. Hui, "Experimental determination of stray capacitances in high frequency transformers," *IEEE Trans. Power Electron.*, vol. 18, no. 5, pp. 1105–1112, Sep. 2003.

[10] J. Smajic *et al.*, "Simulation and measurement of lightning-impulse voltage distributions over transformer windings," *IEEE Trans. Magn.*, vol. 50, no. 2, Feb. 2014, Art. no. 7013604.

[11] T. Zupan, B. Trkulja, R. Obrist, T. Franz, B. Cranganu-Cretu, and J. Smajic, "Transformer windings' RLC parameters calculation and lightning impulse voltage distribution simulation," *IEEE Trans. Magn.*, vol. 52, no. 3, Mar. 2016, Art. no. 8400204.

[12] F. Deleon and A. Semlyen, "Efficient calculation of elementary parameters of transformers," *IEEE Trans. Power Del.*, vol. 7, no. 1, pp. 376–383, Jan. 1992.

[13] B. Cogitore, J. P. Keradec, and J. Barbaroux, "The two-winding transformer: An experimental method to obtain a wide frequency range equivalent circuit," *IEEE Trans. Instrum. Meas.*, vol. 43, no. 2, pp. 364–371, Apr. 1994.

[14] E. Dallago, G. Sassone, and G. Venchi, "High-frequency power transformer model for circuit simulation," *IEEE Trans. Power Electron.*, vol. 12, no. 4, pp. 664–670, Jul. 1997.

[15] P. G. Blanken, "A lumped winding model for use in transformer models for circuit simulation," *IEEE Trans. Power Electron.*, vol. 16, no. 3, pp. 445–460, May 2001.

[16] R. Asensi, R. Prieto, J. A. Cobos, and J. Uceda, "Modeling high-frequency multiwinding magnetic components using finite-element analysis," *IEEE Trans. Magn.*, vol. 43, no. 10, pp. 3840–3850, Oct. 2007.

[17] J. Biela and W. Johann, "Using transformer parasitics for resonant converters—A review of the calculation of the stray capacitance of transformers," *IEEE Trans. Ind. Appl.*, vol. 44, no. 1, pp. 223–233, Jan./Feb. 2008.

[18] Z. De Greve, O. Deblecker, and J. Lobry, "Numerical modeling of capacitive effects in HF multiwinding transformers-Part I: A rigorous formalism based on the electrostatic equations," *IEEE Trans. Magn.*, vol. 49, no. 5, pp. 2017–2020, May 2013.

[19] Z. De Greve, O. Deblecker, and J. Lobry, "Numerical modeling of capacitive effects in HF multiwinding transformers-Part II: Identification using the finite-element method," *IEEE Trans. Magn.*, vol. 49, no. 5, pp. 2021–2024, May 2013.

[20] E. Laveuve, J. P. Keradec, and M. Bensoam, "Electrostatic of wound components: Analytical results, simulation and experimental validation of the parasitic capacitance," in *Proc. Conf. Record IEEE Ind. Appl. Soc. Annu. Meeting*, 1991, vol. 2, pp. 1469–1475.

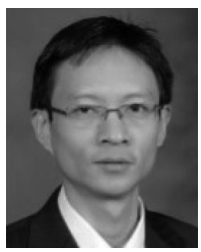
[21] F. Blache, J. P. Keradec, and B. Cogitore, "Stray capacitances of two winding transformers: Equivalent circuit, measurements, calculation and lowering," in *Proc. Ind. Appl. Soc. Annu. Meeting.*, 1994, vol. 2, pp. 1211–1217.

[22] L. Dalessandro, F. D. Cavalcante, and J. W. Kolar, "Self-capacitance of high-voltage transformers," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 2081–2092, Sep. 2007.

[23] S. Wang, P. J. Kong, and F. C. Lee, "Common mode noise reduction for boost converters using general balance technique," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1410–1416, Jul. 2007.

Huan Zhang received the B.S. and M.S. degrees in electrical engineering from Huazhong University of Science and Technology, Wuhan, China, in 2008 and 2011, respectively. He is currently working toward the Ph.D. degree in electrical engineering from the Department of Electrical and Computer Engineering, University of Florida, Gainesville, FL, USA.

From 2011 to 2014, he was an Electrical Engineer in Guangdong Electric Power Design Institute, Guangzhou, China. His research interests include power conversion systems and electromagnetic interference.



Shuo Wang (S'03–M'06–SM'07) received the Ph.D. degree in electrical engineering from Virginia Tech, Blacksburg, VA, in 2005.

Since 2015, he has been an Associate Professor in the Department of Electrical and Computer Engineering, University of Florida, Gainesville, FL. From 2010 to 2014, he was with the University of Texas, San Antonio, TX, first as an Assistant Professor and later as an Associate Professor. From 2009 to 2010, he was a Senior Design Engineer with GE Aviation Systems, Vandalia, OH. From 2005 to 2009, he was a Research Assistant Professor with Virginia Tech. He has published more than 130 IEEE journal and conference papers and holds 8 US patents.

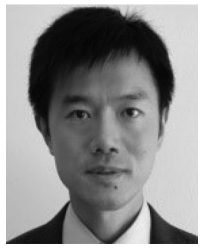
Dr. Wang received the Best Transaction Paper Award from the IEEE Power Electronics Society in 2006 and two William M. Portnoy Awards for the papers published in the IEEE Industry Applications Society in 2004 and 2012, respectively. In 2012, he received the prestigious National Science Foundation CAREER Award. He is an Associate Editor for the IEEE Transactions on Industry Applications and a technical program Co-Chair for the IEEE 2014 International Electric Vehicle Conference.

Yiming Li (S'16) received the B.S.E.E. degree in electrical engineering from Zhejiang University, Zhejiang, China, in 2015. He is currently working toward the Ph.D. degree in electrical engineering at University of Florida, Gainesville, FL, USA.

His research interests include electromagnetic interference/electromagnetic compatibility in power electronic systems, transformer design for isolated converters, and filter design in power electronic devices.

Qinghai Wang received the B. Eng. degree in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2001.

After graduation, he has been with Huawei Technologies co., Ltd, where he was involved in EMC and surge protection design and research for ICT and power module. He is currently a Chief Design Engineer and the Leader of EMC and Lightning Technology Manage Group. He had made outstanding contributions to protection circuit design, the miniaturization of protection and filter circuits, LF filter design and grounding design etc. His current research interest includes EMI modeling and system simulation, EMI suppression, passive and active filter design for power electronic product. He is a member of several standard organizations and has been responsible for the constituting of several standards. He holds 12 patents.



Dianbo Fu received the B.S. degree in electrical engineering from Huazhong University of Science and Technology, Wuhan, China, and the M.S. and Ph.D. degrees in electrical engineering from Virginia Polytechnic Institute and State University, respectively.

In 2010, he was with Huawei Technologies, Plano, TX, where he has been engaged in product design, research and development. His research interests include high-frequency power conversion, soft switching techniques, magnetic design, EMI, telecom power conversion, and power inversion techniques. He holds 24 U.S. patents, and has 21 U.S. patents pending.

Dr. Fu received the William M. Portnoy Award from the IEEE Industry Applications Society in 2012.